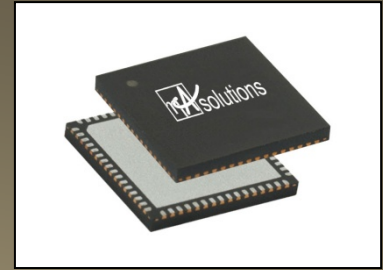


NS2213-15

Delta-Sigma Fractional-N Synthesizer

All Digital Phase Locked Loop



Features

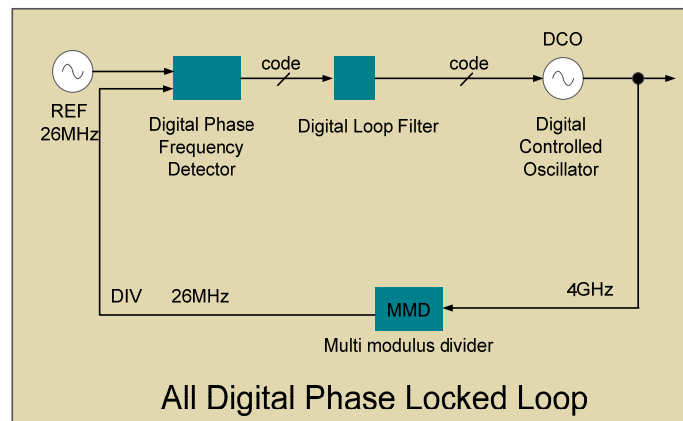
- 2.9 to 4.2GHz Operation
- Reference frequency of 26MHz
- Phase noise -145 dbc/Hz at 20MHz offset at 4 GHz
- Spurious response -95 dBc
- 65nm digital CMOS process
- Ultra low deep-sleep mode current
- 65nm mixed-signal CMOS technology
- Integrated $\Sigma-\Delta$ synthesizer, VCO, and loop filter
- Single supply operation at 1.2V

Benefits

- Silicon proven design
- Ultra-low power consumption with 15 mA at 1.2V
- Small silicon footprint at 1 sq mm
- Scalable 65 nm CMOS eliminates external components

Applications

- WCDMA
- WiMax
- Wifi



Description

The NanoAmp Solutions delta-sigma fractional-N frequency synthesizer is a 65nm CMOS implementation of an all digital phase locked loop (ADPLL). It can be used in the construction of a local oscillator for a WCDMA wireless transceiver. The NanoAmp delta-sigma fractional-N frequency synthesizer is both ultra low power and high precision, with low phase noise and low spurious response for applications requiring low adjacent or alternate channel interference. The cell operates using 15mA from a 1.2V supply, with an output of 2.9 to 4.2GHz and a temperature of 85°C.

Electrical Characteristics

Parameter	Conditions	Min	Typ	Max	Units
Supply Voltage			1.2		V
Total Supply Current			15		mA
RF Input Operating Frequency		2.9		4.2	GHz
Reference Oscillator Frequency			26 MHz		
Charge Pump Variation Over Temperature	All digital		None		
Synthesizer contribution to close-in Phase Noise			-80		dBc/Hz
Phase Noise 1MHz			-118		dBc/Hz
Phase Noise 20MHz			-145		dBc/Hz
Phase Noise 45MHz			-152		dBc/Hz
Phase Noise 80MHz			-157		dBc/Hz
Frequency Resolution		2			kHz/bit LSB
Operating Temperature		-40		85	

Legend

O = Output
 I = Input
 IO = Input/Output
 P = Power (Supply or Ground)
 A = Analog Signal